



**GURU GOBIND SINGH INDRAPRASTHA UNIVERSITY,  
EAST DELHI CAMPUS,  
SURAJMAL VIHAR-110092**

|   |          |            |                |
|---|----------|------------|----------------|
| <b>Semester: 3<sup>rd</sup></b>           |          |            |                |
| <b>Paper code: AIDS205/AIML205/IOT205</b> | <b>L</b> | <b>T/P</b> | <b>Credits</b> |
| <b>Subject: Digital Logic Design</b>      | <b>3</b> | <b>0</b>   | <b>3</b>       |
| <b>Marking Scheme</b>                     |          |            |                |

1. Teachers Continuous Evaluation: As per university examination norms from time to time
2. End term Theory Examination: As per university examination norms from time to time

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| <b>INSTRUCTIONS TO PAPER SETTERS: Maximum Marks:</b> As per university norms   |
| <ol style="list-style-type: none"> <li>1. There should be 9 questions in the end term examination question paper</li> <li>2. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions.</li> <li>3. Apart from Question No. 1, the rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, students may be asked to attempt only 1 question from each unit.</li> <li>4. The questions are to be framed keeping in view the learning outcomes of course/paper. The standard/ level of the questions to be asked should be at the level of the prescribed textbooks.</li> <li>5. The requirement of (scientific) calculators/ log-tables/ data-tables may be specified if required.</li> </ol> |

**Course Objectives:**

|    |  |
|----|--|
| 1. | To teach various number systems, binary codes and their applications.                          |
| 2. | To familiarize the students with the importance of error detection and error correction codes. |
| 3. | To inculcate concepts of K-MAP to simplify a Boolean expression.                               |
| 4. | To facilitate students in designing a logic circuit.   |

**Course Outcomes:**

|            |   |
|------------|---|
| <b>CO1</b> | Understand number systems and complements for the basic functionality of digital systems  |
| <b>CO2</b> | Identify the importance of canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits. |
| <b>CO3</b> | Apply and evaluate circuits of minimizing algorithms (Boolean algebra, Karnaugh map or tabulation method).                                |
| <b>CO4</b> | Design procedures of combinational and sequential circuits.   |

| CO/PO | PO01 | PO02 | PO03 | PO04 | PO05 | PO06 | PO07 | PO08 | PO09 | PO10 | PO11 | PO12 |
|-------|------|------|------|------|------|------|------|------|------|------|------|------|
| CO1   | 2    | 2    | 2    | 2    | 1    | -    | -    | -    | -    | -    | -    | 1    |
| CO2   | 2    | 2    | 2    | 2    | 1    | -    | -    | -    | -    | -    | -    | 1    |
| CO3   | 2    | 2    | 2    | 2    | 1    | -    | -    | -    | -    | -    | -    | 1    |
| CO4   | 2    | 2    | 2    | 2    | 1    | -    | -    | -    | -    | -    | -    | 1    |

**Course Overview:**



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The course addresses the concepts of digital systems logic design, and techniques of designing digital systems. The course teaches the fundamentals of digital systems applying the logic design and development techniques. This course forms the basis for the study of advanced subjects like Computer Organization and Architecture, Microprocessor through Interfacing, VLSI Designing.

**UNIT I:** [8]  
**Digital systems**, binary numbers, number base conversions, octal and hexadecimal numbers, complements, signed binary numbers, binary codes, error detection and error correction codes. Boolean Algebra and Logic Gates: Basic definitions, axiomatic definition of Boolean algebra, basic theorems and properties of Boolean algebra, Boolean functions, canonical and standard forms, other logic operations, digital logic gates.

**UNIT II:** [8]  
**GATE level minimization**, Logic gates and Logic families, The K-map method, four-variable map, five-variable map, product of sums simplification, don't-care conditions, NAND and NOR implementation, determination and selection of Prime Implicants, Essential and Nonessential prime Implicants.

**UNIT III:** [8]  
**Combinational logic and their Design procedure**, Binary Adder, Binary Subtractor, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers, and Demultiplexers.  
Memories such as ROM, RAM, EPROM.

**UNIT IV:** [12]  
**Sequential logic and circuits**, latches, flip-flops, analysis of clocked sequential circuits, State reduction and assignment, design procedure. **REGISTERS AND COUNTERS:** Registers, shift registers, ripple counters, synchronous counters, counters with unused states, ring counter, Johnson counter. Random access memory, memory decoding, error detection and correction, read only memory, programmable logic array, programmable array logic, sequential programmable devices. A/D and D/A converters.

**Text Books:**

1. M. Morris Mano, Michael D. Ciletti (2008), Digital Design, 4th edition, Pearson Education Inc, India.
2. Donald D. Givone (2002), Digital Principles and Design, Tata McGraw Hill, India.

**Reference Books:**

1. C. V. S. Rao (2009), Switching and Logic Design, 3rd Edition, Pearson Education, India.
2. Roth (2004), Fundamentals of Logic Design, 5th Edition, Thomson, India.